UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,816	08/21/2002	Hou-Yuan Lin	GIGP0001USA	7780

27765 7590 06/09/2005

NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
PEUGH, BRIAN R	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,816	LIN, HOU-YUAN	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/1/05,2/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed December 8, 2004 in response to PTO Office Action dated June 12, 2002. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-8 have been presented for examination in this application. In response to the last Office Action, claim 8 has been added.

Please note the change in Patent Examiner assigned to the current Application.

Information Disclosure Statement

The information disclosure statement (IDS) originally submitted on February 18, 2005 is not being considered by the Examiner due to illegibility of the document. The IDS of March 1, 2005, which is a legible copy of the IDS of February 18, 2005, is in compliance with the provisions of 37 CFR 1.97. Accordingly, this information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA) in view of Klein (US# 6,349,051).

In regards to the previous Office Action for claims 1-7, the rejections attributed to claims 1-7 below has been expanded upon by the Examiner in the interest of increased clarity for the Applicant. No new references or rejections have been made. A new rejection for newly entered claim 8 has been added.

Regarding claims 1 and 8, AAPA teaches **a basic input/output (BIOS) for storing an access control program and outputting a control signal when the access control program is activated** (col. 1, para. 0007; Fig. 1-3; BIOS also described in para. 0022]; **a chipset connected to the BIOS for receiving the control signal** [Fig. 1-3]; **a dynamic random access memory (DRAM) module socket comprising three access control mode input ports** [Fig. 1-3].

The prior art of Fig. 1, for example, fails to teach that the integrated chipset has a pair of general purpose input/output (GPIO) terminals for outputting a first and second control output', and a pair of switches for respectively receiving the first access control signal and the second access control signal and selectively outputting the first access control signal and the second access control signal to the three access control mode

input ports respectively according to the first control output and the second control output.

Klein in Fig. 4 teaches the use of a bus switch, controlled by a control input, as to connect its input data bus to one of its output data buses. This bus switch is situated between a memory controller, which supplies the control input, and a memory module.

Klein teaches that the switch (27) of Figure 4 includes the interface circuitry (26) in Figure 3 [col. 4, lines 57-63]. Although the switch in Figure 4 is identified as (33), the Examiner will interpret the Klein reference according to the switch (33) of Figure 4 including the interface circuitry (26) of Figure 3. Interface circuitry (26) of Figure 3 includes two switches, where each switch is coupled to the memory controller via the same data bus (30a,30b), and where each bus is coupled to a separate data bus (30c; 30d) in which to transport data out of the switch. In reference to Figure 3, Klein teaches that additional circuitry including control buses connect host processor (20) with memory controller (22) [col. 4, lines 1-4]. Klein also teaches that with the two switches (identified as 32a & 32b in the disclosure; identified as 32a and 22b in Figure 3), it can be appreciated that by turning the switches 32a and 32b on or off, one or the other memory circuit 28 may be removed from the data bus [col. 4, lines 16-22]. Therefore, Klein contemplates the inclusion of control signals as well as being able to turn the switches on or off in order to direct data to one of the two circuits.

Since Klein has indicated that the switch of Figure 4 includes the interface circuitry of Figure 3, then the switch (33) of Figure 4 in fact incorporates two separate switches. Klein teaches that the memory controller (23) outputs control output (37)

which controls bus switch (27) [33] in order to route the data bus (31a) to one of the memory modules [col. 5, lines 9-13]. Although not explicitly recited by Klein, the control output (27) would inherently be required by the two switches incorporated within switch (33) for the proper routing of data. Thus, the control output (37) would be required to connect to both switches separately as first and second control signal buses. Therefore, Klein teaches a pair of [general purpose input/output (GPIO)] terminals for outputting a first and second control output, and a pair of switches (32a & 32b) for respectively receiving the first access control signal and the second access control signal and selectively outputting the first access control signal and the second access control signal to the three access control mode input ports respectively according to the first control output and the second control output [Figure 4 of Klein illustrates four separate memory input ports, which corresponds to the input ports as required by the claimed DRAM for receiving data signals.

It would be obvious to one of ordinary skill in the art at the time the invention was made to insert the switching device of Klein having a reasonable number of switches (e.g. one or two) in the data path of the access control mode input ports of the memory module socket of the AAPA in order to reduce the parasitic capacitance of the data bus and increase the speed of data transfer (Klein col. 2 lines 52-54). It follows that this modification would necessitate control signals for the switching device. It is common practice in the art to use the GPIO terminals of many commercially available integrated chipsets to provide these control signals.

Regarding claim 2, the admitted prior art in Fig. 1 discloses **an integrated chipset** that receives the control signal from BIOS access control program.

Regarding claim 3, the admitted prior art in Fig. 1 discloses **a pair of access control mode output pods that are an Error Correction Code (ECC)/Clock Enable (CKE) mode output pod and a Data Input Output Mask (DQM)/CKE mode output port**.

Regarding claim 4, the admitted prior art in Fig. 1 fails to teach **a DRAM module socket that is a DDRDRAM socket**. As it is common practice in the art, it would be obvious to a person of ordinary skill in the art at the time the invention was made to use a commercially available DDRDRAM socket for high data rate memory applications.

Regarding claim 5, the admitted prior art in Fig. 1 fails to teach **a DRAM module socket that is a RDRAM socket**. As it is common practice in the art, it would be obvious to a person of ordinary skill in the art at the time the invention was made to use a commercially availableRDRAM socket for high data rate memory applications.

Regarding claim 6, the admitted prior art in Fig. 1 discloses that the **three access control mode input ports are an EEC mode input port, a CKE mode input port and a DQM mode input port**.

Regarding claim 7, the admitted prior art in Fig. 1 fails to teach the use of **switches that respectively receive the first control output and the second control output to selectively output the first access control signal and the second access control signal to two of the three access control mode input ports.**

This further claimed limitation of selective output to "two of the three access control mode input ports" would follow necessarily when the admitted prior art device is modified in the manner mentioned in the rejection of claim 1. It was been known and commonly practiced in the pertinent art to use a switching device to selectively couple data buses in a combinatorial manner in accordance with the rejection for claim 1 as disclosed supra.

Response to Arguments

Applicant's arguments filed December 8, 2004 have been fully considered but they are not persuasive.

The Examiner has expanded upon the previous 35 U.S.C. 103 rejection in order to better detail the teachings of Klein and how the teachings apply to Applicant's claimed subject matter.

Applicant has described the Klein reference on pages 5-6 of the response, while articulating Applicant's switch system on pages 6-7. Applicant has argued on page 7, paragraph one that the "... present invention management system utilizes software to directly control a desired combination of the access control modes for a DRAM module,

and thus does not require any physical reconfiguration of the hardware of the motherboard to effect such access control mode reconfiguration (Paragraph [0026]). With this in mind, it is difficult for the Applicant to understand how the suggested Klein motive of installing a switch to reduce parasitic capacitance and thereby speed data transfers could possibly apply to the admitted prior art. Because the admitted prior art requires physical reconfiguration of the hardware to enable the appropriate data bus for the desired configuration, via jumpers or otherwise, it would seem obvious that the buses not required for a specific configuration are not enabled, unless user enabled by the physical hardware change. Therefore, the admitted prior art already reduces parasitic capacitance as effectively and in much the same manner as the switch of Klein by necessitating the physical reconfiguration of the hardware. Thus, there is no reason for a suggested combination that merely results in unwanted and unnecessary redundancy."

The Examiner has included the Klein reference in order to teach the claim limitations directed towards routing data (regardless of type) to specific inputs based on control signals (regardless of type). The Klein reference teaches that the switches are governed according to control signals, as disclosed above. This idea of data movement based on control signal applied switches is akin to Applicant's invention, in that Applicant's invention has improved upon Applicant's prior art by adding switches between the control signal outputs and the data destination inputs. In its most basic form, the switches of Applicant's invention are used to route the data (ECC/CKE and DQM/CKE) signals from the chipset outputs to the DRAM memory (ECC, CKE, and

DQM) inputs via the control signals (from the GPIO outputs). The invention of Klein performs in the same way, in that the data is routed from a memory controller to the memory inputs according to the control signals inputted to the switches. Although the Klein reference does not teach inserting switches so as to not require any physical reconfiguration of the hardware of the motherboard to effect such access control mode reconfiguration, Klein has taught that the use of the switches will reduce the parasitic capacitance and increase bus speeds as disclosed above. Applicant's disclosure has not made mention of parasitic capacitance as a problem to be corrected by including control signal operated switches, but rather to use the switches to prevent possible hardware reconfiguration. The Klein reference teaches incorporating the switches to produce the same result for other reasons, as well as teaching all of the necessary switch claim limitations, as recited above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to related DRAM systems.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Patent Examiner
Art Unit 2187
May 20, 2005